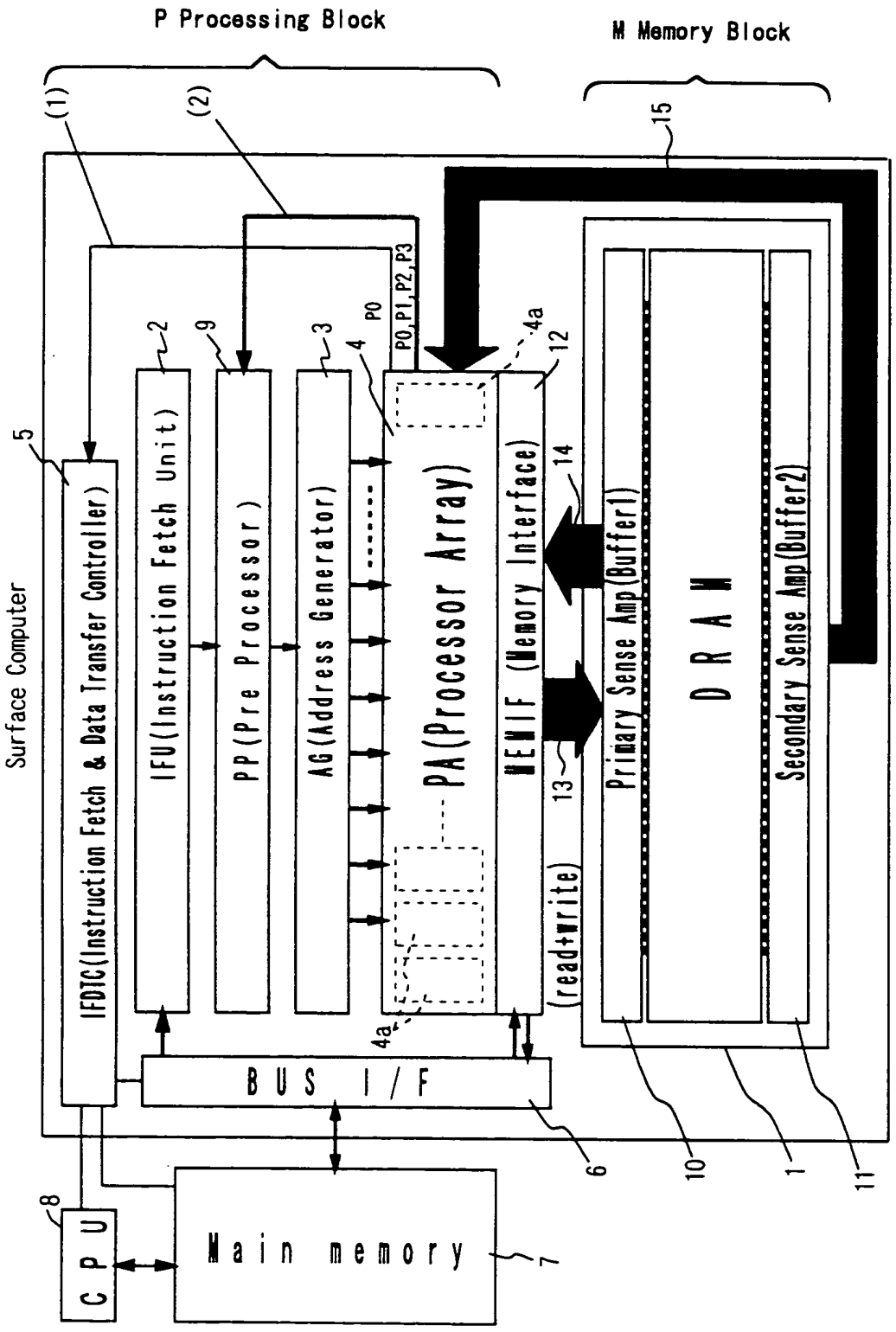

P Processing Block
M Memory Block
(1)
(2)
15
Surface Computer
5
IFDTC(Instruction Fetch & Data Transfer Controller)
IFU(Instruction Fetch Unit)
2
9
PP(Pre Processor)
AG(Address Generator)
3
4
P0
P0,P1,P2,P3
PA(Processor Array)
4a
MEMIF (Memory Interface)
12
14
13
(read+write)
Primary Sense Amp(Buffer1)
DRAM
Secondary Sense Amp(Buffer2)
BUS I/F
6
10
1
11
8
CPU
Main memory
7

FIG. 1

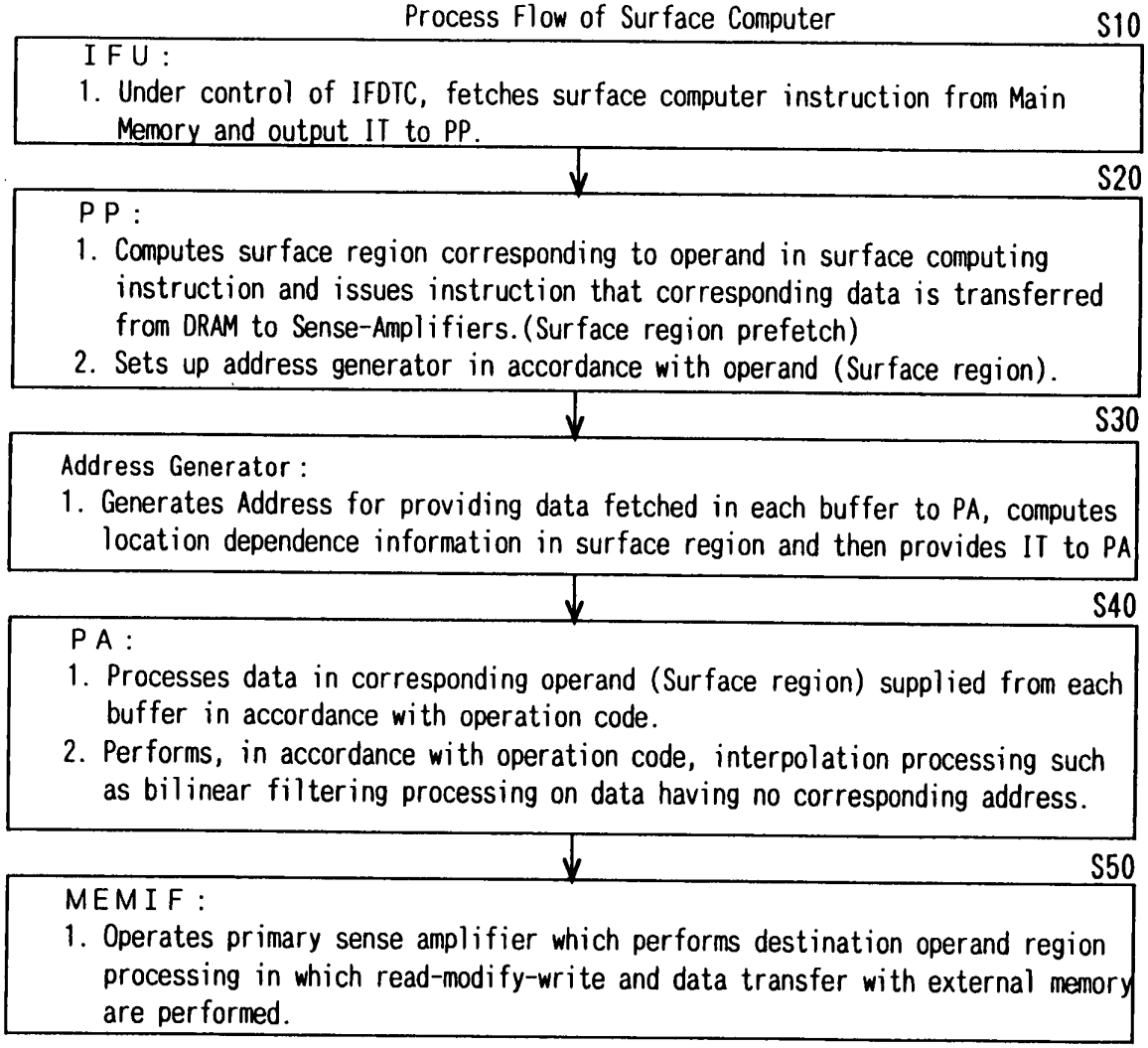

Process Flow of Surface Computer
S10
IFU :
1. Under control of IFDTC, fetches surface computer instruction from Main Memory and output IT to PP.
S20
PP :
1. Computes surface region corresponding to operand in surface computing instruction and issues instruction that corresponding data is transferred from DRAM to Sense-Amplifiers.(Surface region prefetch)
2. Sets up address generator in accordance with operand (Surface region).
S30
Address Generator :
1. Generates Address for providing data fetched in each buffer to PA, computes location dependence information in surface region and then provides IT to PA
S40
PA :
1. Processes data in corresponding operand (Surface region) supplied from each buffer in accordance with operation code.
2. Performs, in accordance with operation code, interpolation processing such as bilinear filtering processing on data having no corresponding address.
S50
MEMIF :
1. Operates primary sense amplifier which performs destination operand region processing in which read-modify-write and data transfer with external memory are performed.

FIG. 2

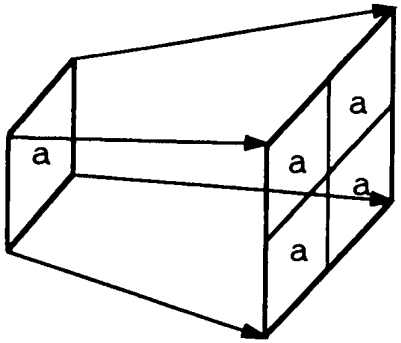


FIG. 3A

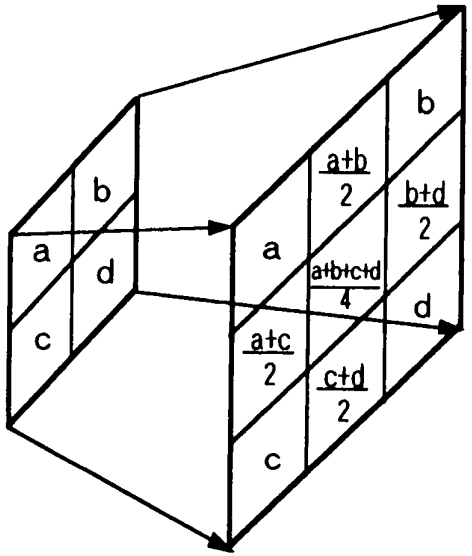


FIG. 3B

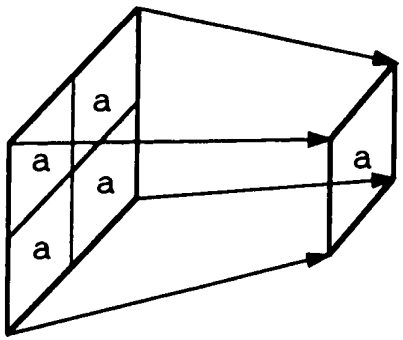


FIG. 4A

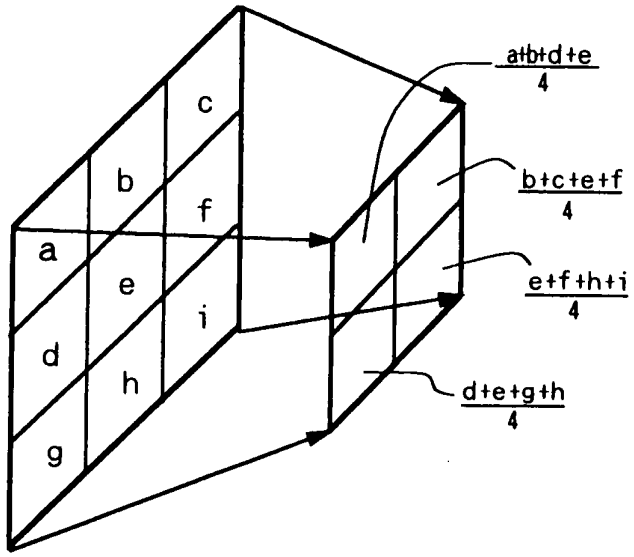


FIG. 4B

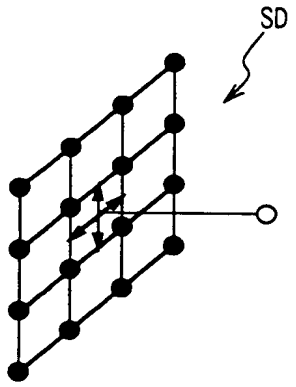


FIG. 5A

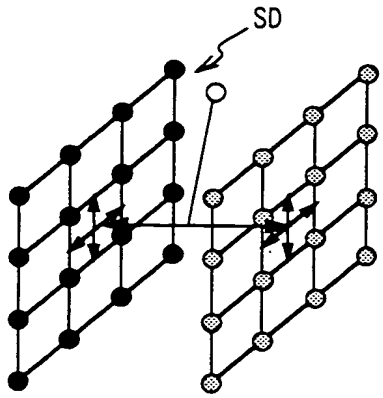


FIG. 5B

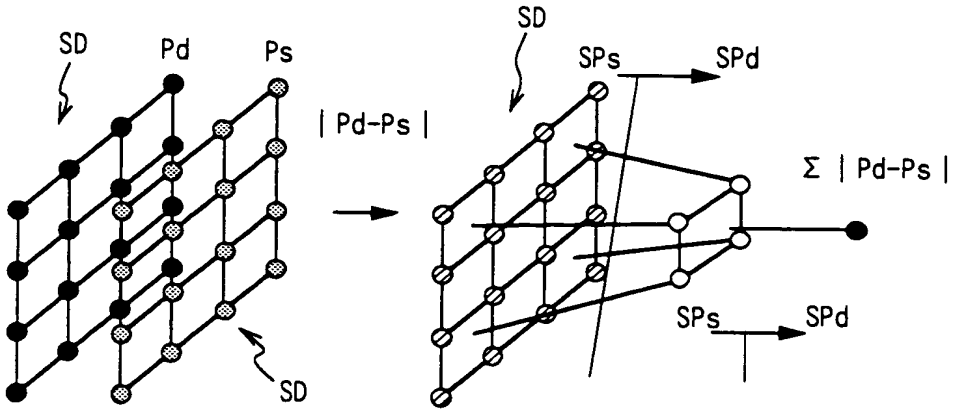
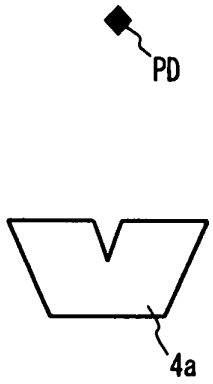
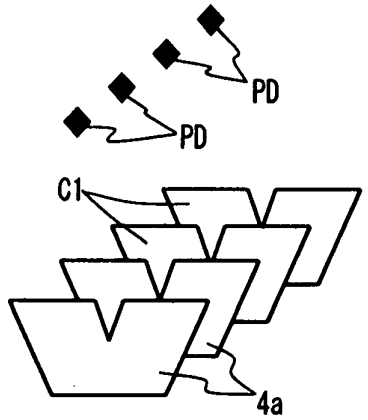


FIG. 6



PRIOR ART

FIG. 7A



PRIOR ART

FIG. 7B

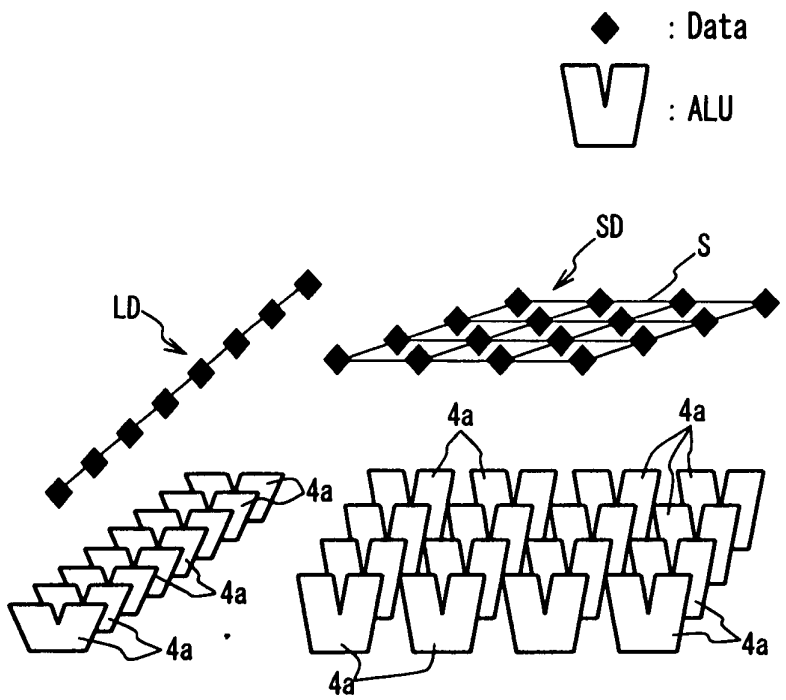
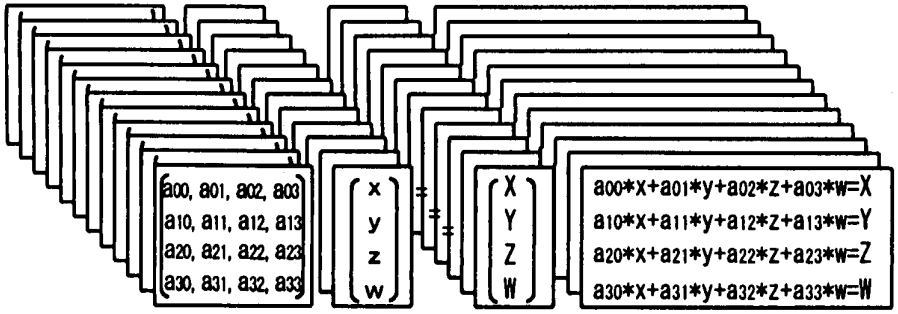
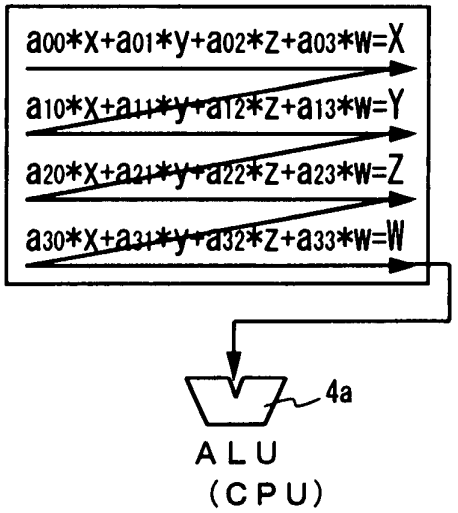


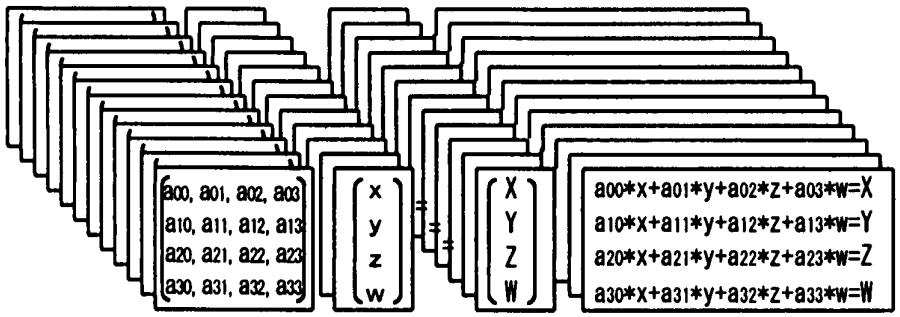
FIG. 7C

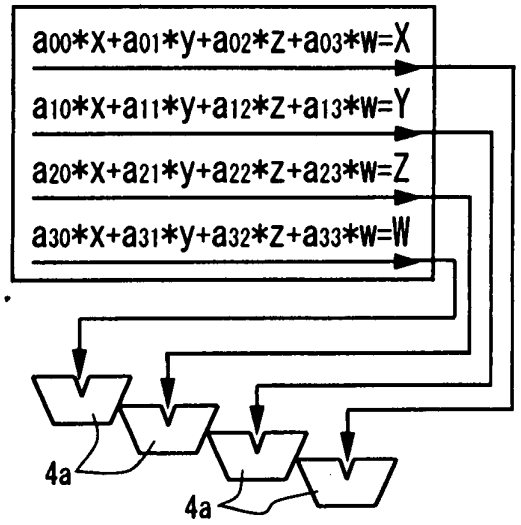




PRIOR ART

FIG. 8





PRIOR ART

FIG. 9

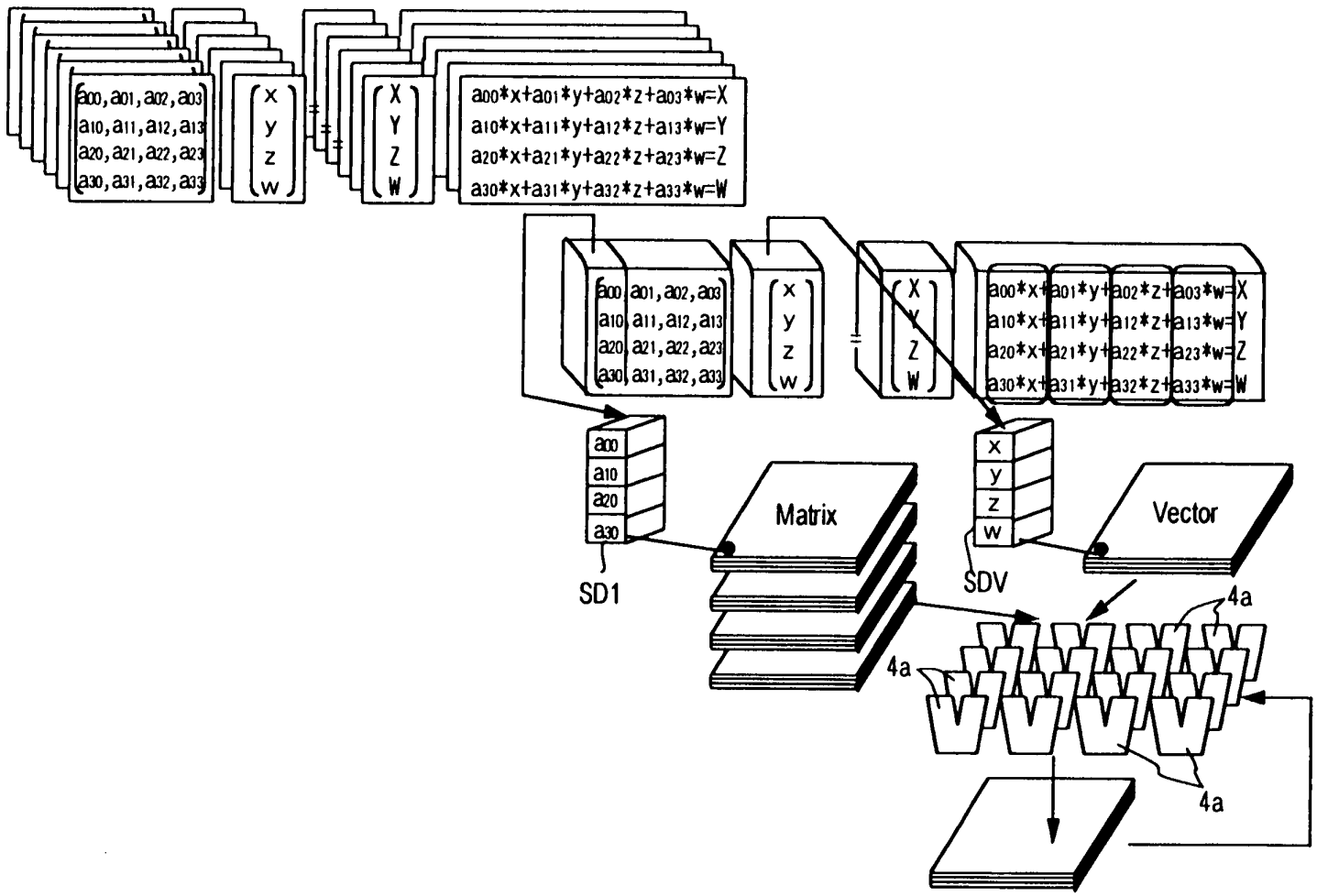

a00, a01, a02, a03
a10, a11, a12, a13
a20, a21, a22, a23
a30, a31, a32, a33
x
y
z
w
X
Y
Z
W
a00*x+a01*y+a02*z+a03*w=X
a10*x+a11*y+a12*z+a13*w=Y
a20*x+a21*y+a22*z+a23*w=Z
a30*x+a31*y+a32*z+a33*w=W
a00
a10
a20
a30
SD1
Matrix
SDV
Vector
4a
4a
4a

FIG. 10

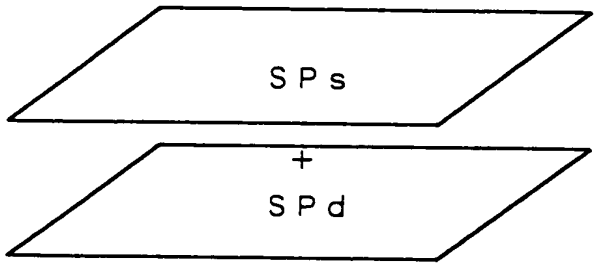


FIG. 11

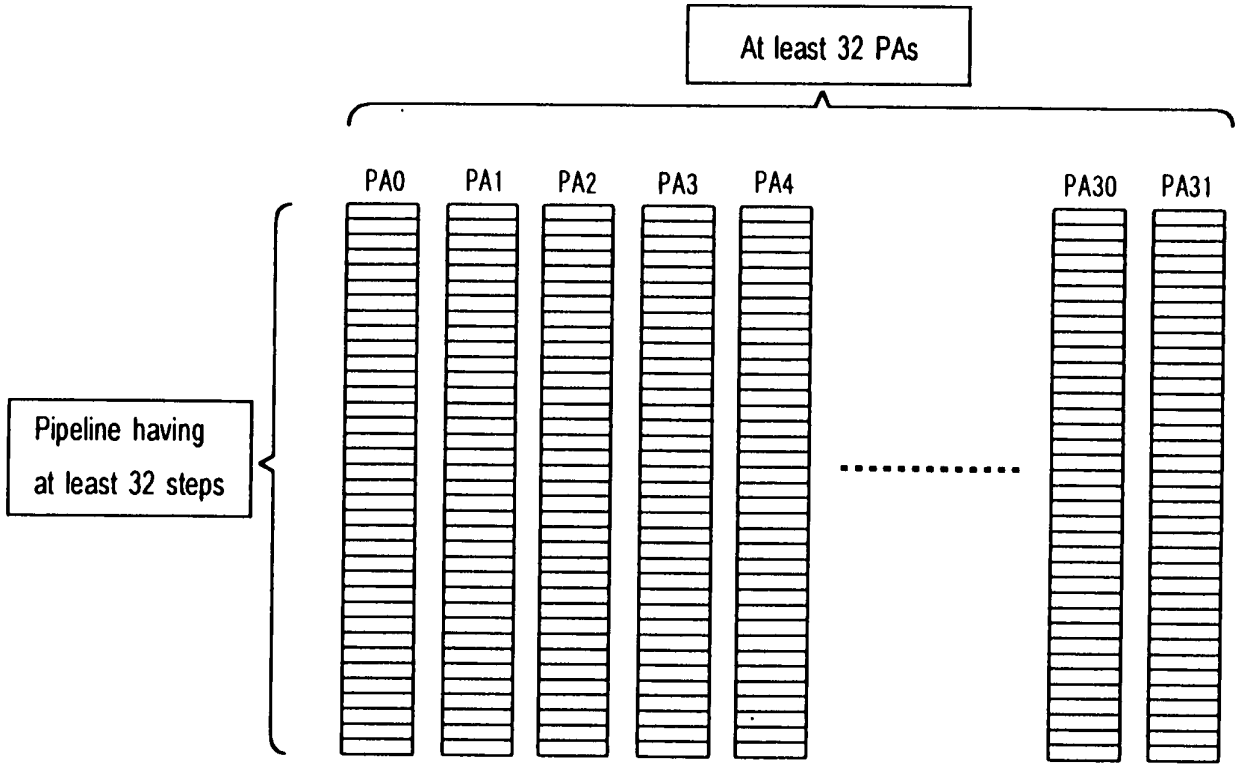
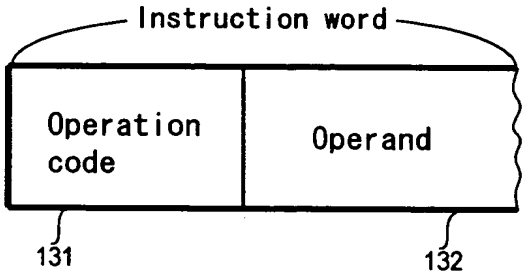

At least 32 PAs
PA0
PA1
PA2
PA3
PA4
PA30
PA31
Pipeline having
at least 32 steps

FIG. 12



PRIOR ART

FIG. 13A

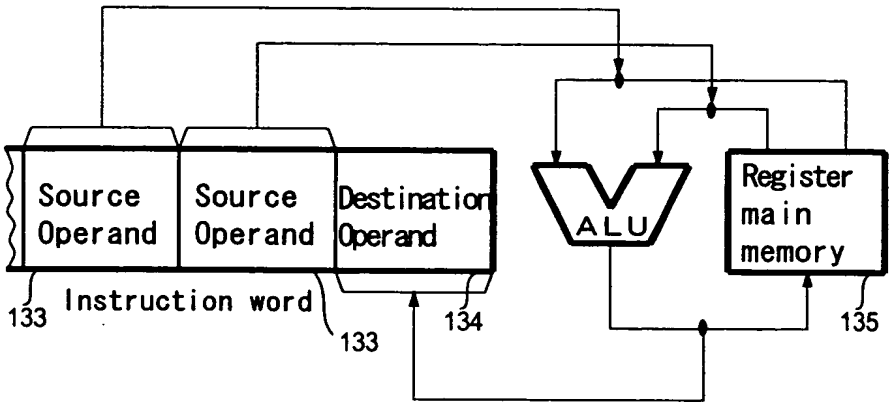


FIG. 13B

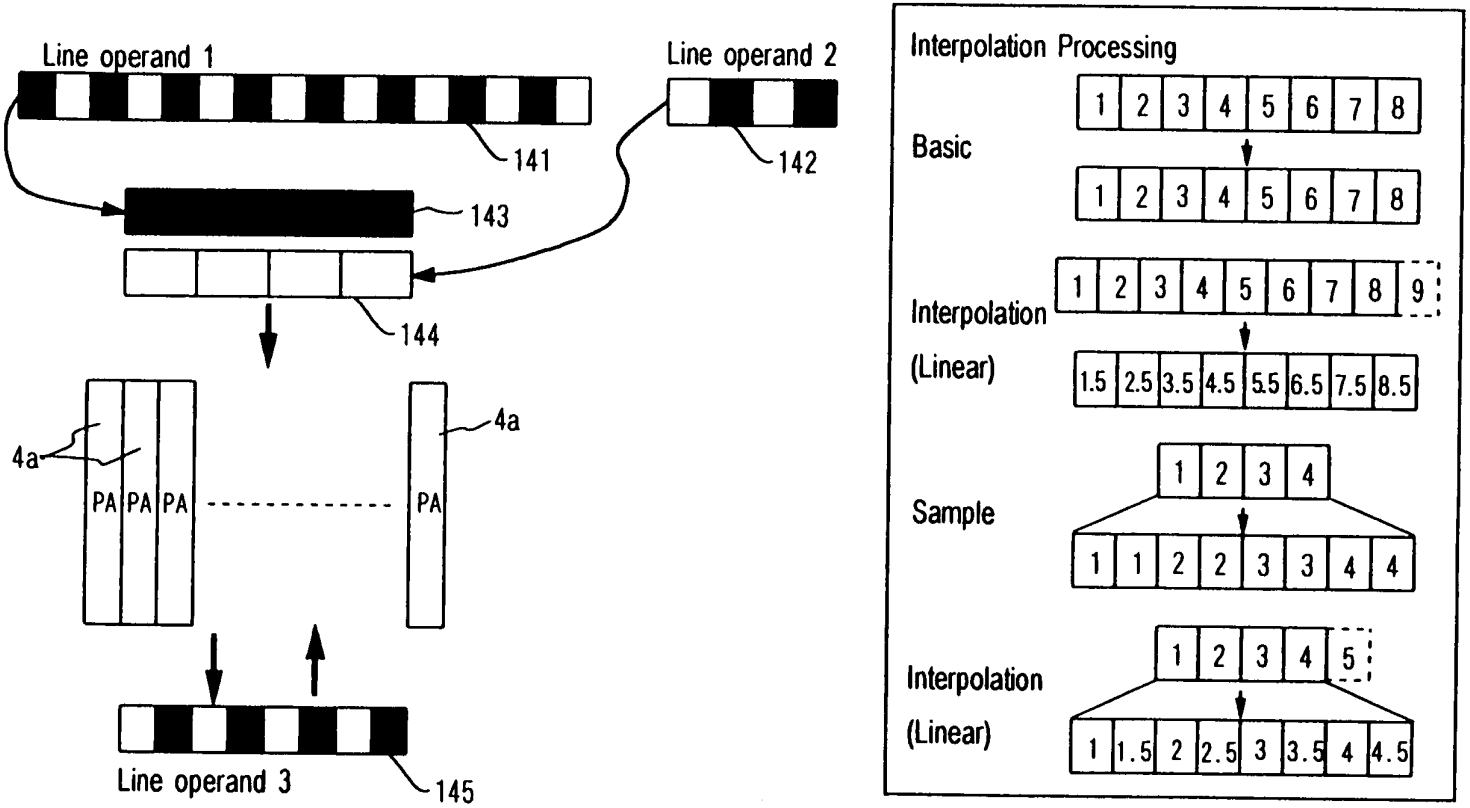

Line operand 1
Line operand 2
141
142
143
144
4a
4a
PA PA PA
PA
Line operand 3
145
Interpolation Processing
Basic
1 2 3 4 5 6 7 8
1 2 3 4 5 6 7 8
Interpolation
(Linear)
1 2 3 4 5 6 7 8 9
1.5 2.5 3.5 4.5 5.5 6.5 7.5 8.5
Sample
1 2 3 4
1 1 2 2 3 3 4 4
Interpolation
(Linear)
1 2 3 4 5
1 1.5 2 2.5 3 3.5 4 4.5

FIG. 14

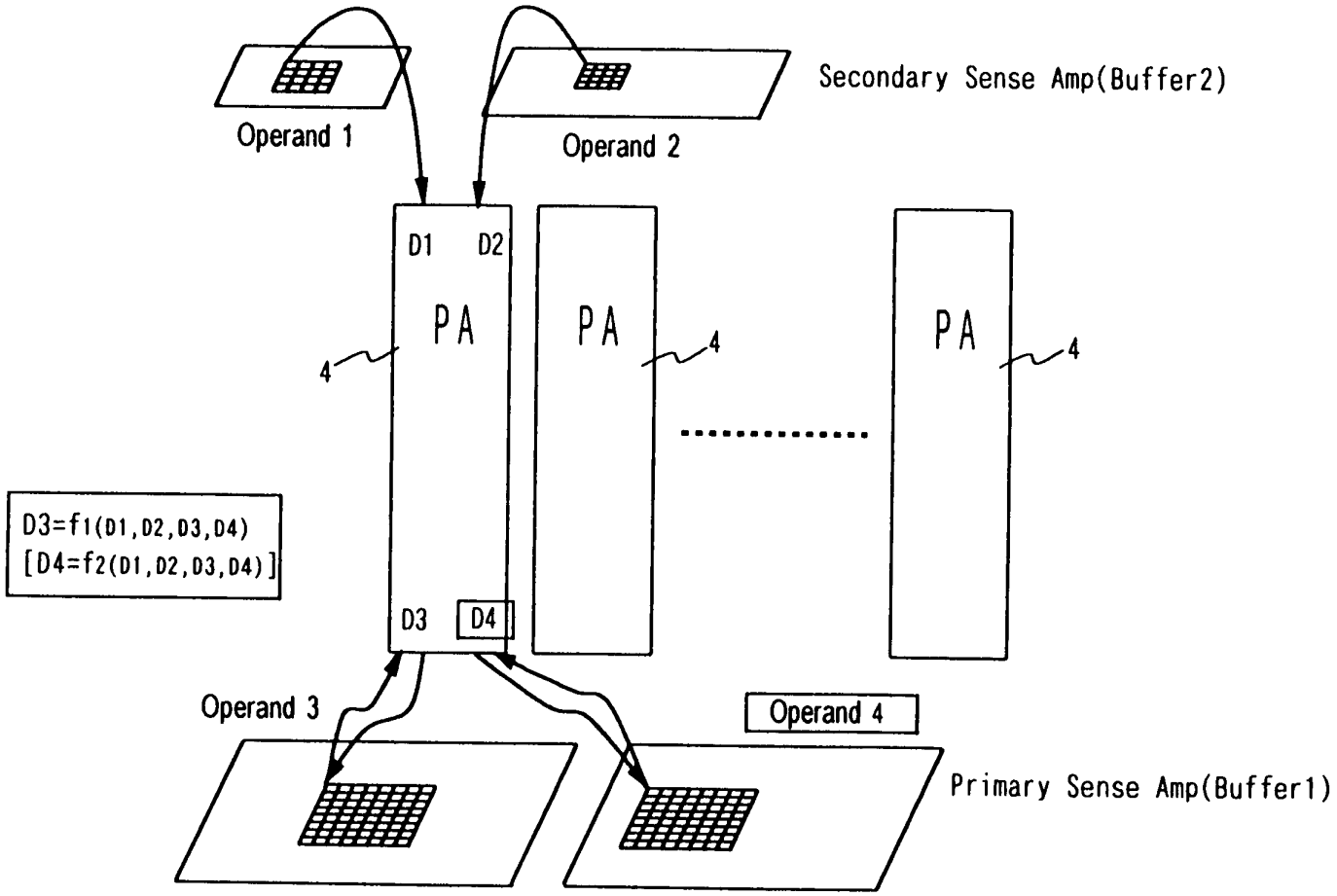

Operand 1
Operand 2
Secondary Sense Amp(Buffer2)
D1
D2
PA
PA
PA
4
4
4
D3=f1(D1,D2,D3,D4)
[D4=f2(D1,D2,D3,D4)]
D3
D4
Operand 3
Operand 4
Primary Sense Amp(Buffer1)

FIG. 15

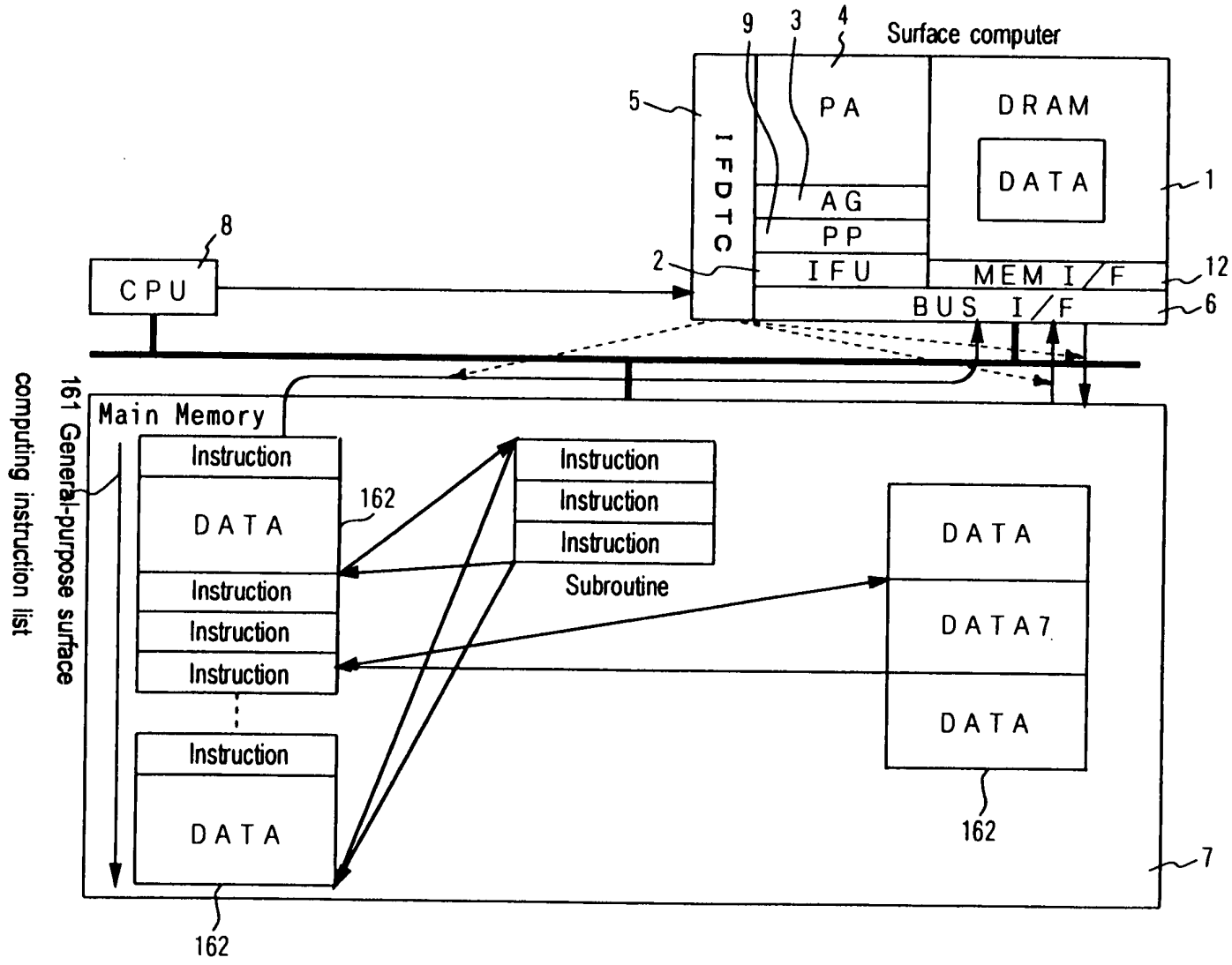

9
3
4
Surface computer
5
IFDTC
PA
DRAM
DATA
1
AG
PP
2
IFU
MEM I/F
12
BUS I/F
6
8
CPU
Main Memory
161 General-purpose surface computing instruction list
Instruction
DATA
162
Instruction
Instruction
Instruction
Instruction
Subroutine
Instruction
Instruction
Instruction
DATA
DATA7
DATA
162
Instruction
DATA
162
7

FIG. 16

(1)

```
Move    IF-Register0,PTs          //Move coordinates of point to IF-Register0
 :
 :
BEQ     IF-Register0,0,label1  //IF-Register0=0 then jump to label 1
```

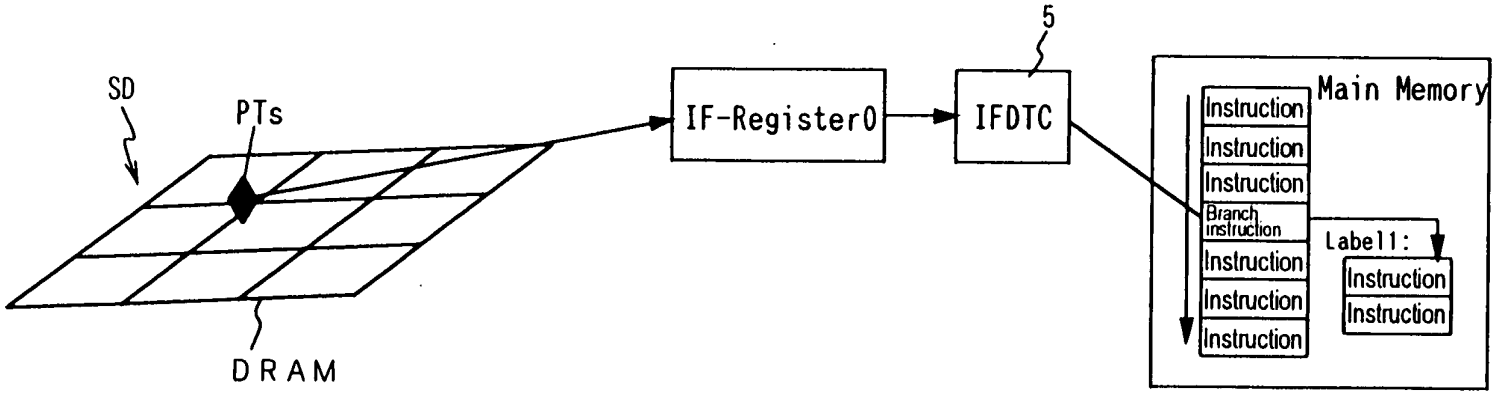


FIG. 17

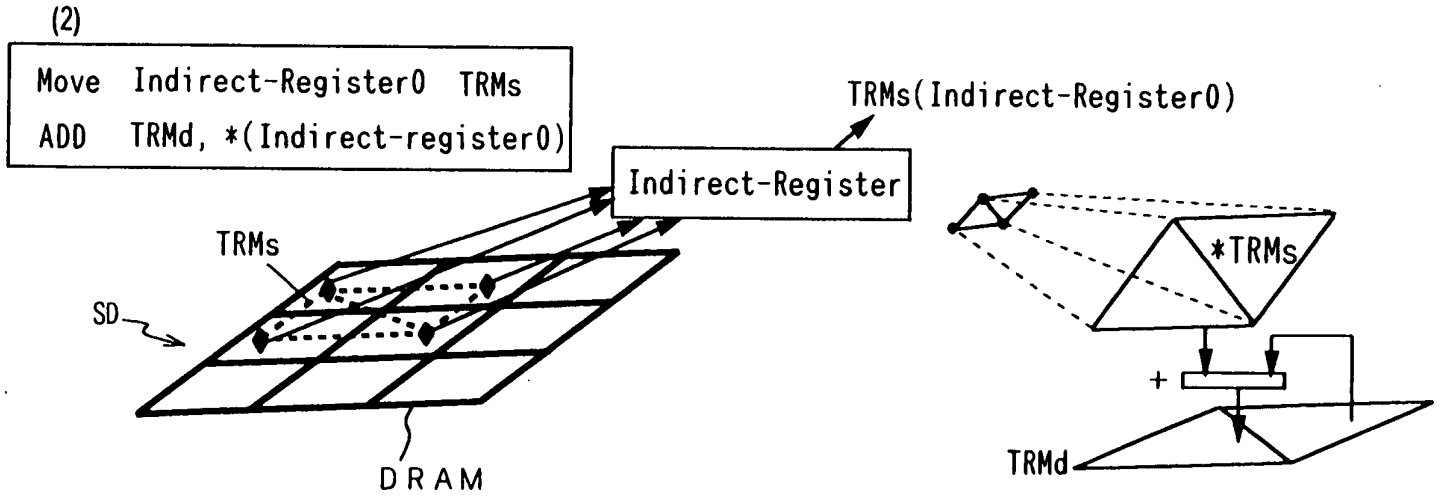

(2)
Move Indirect-Register0 TRMs
ADD TRMd, *(Indirect-register0)
TRMs(Indirect-Register0)
Indirect-Register
TRMs
SD
DRAM
*TRMs
+
TRMd

FIG. 18

FIG. 19A

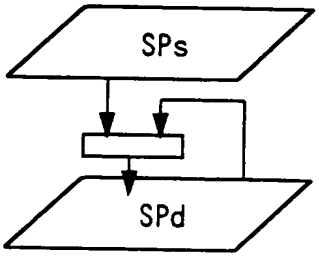


FIG. 19B

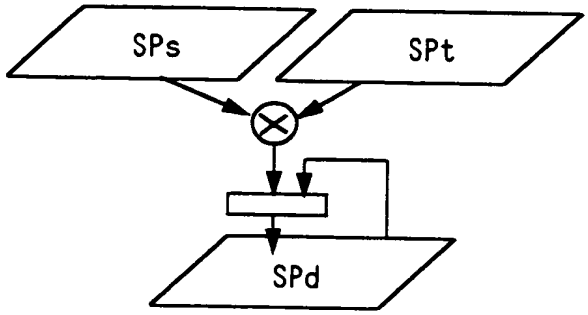


FIG. 19C

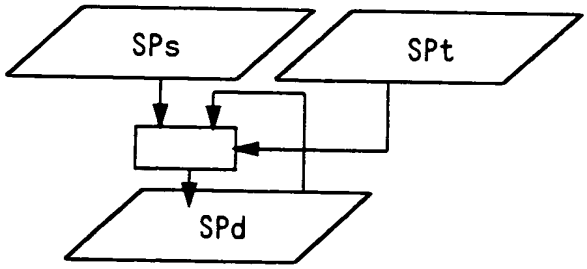
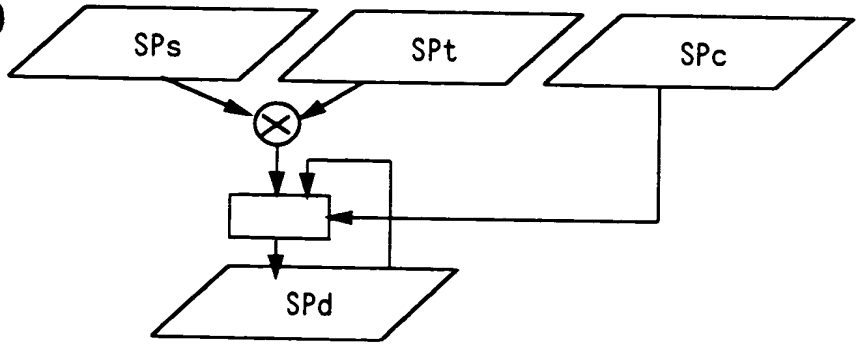


FIG. 19D



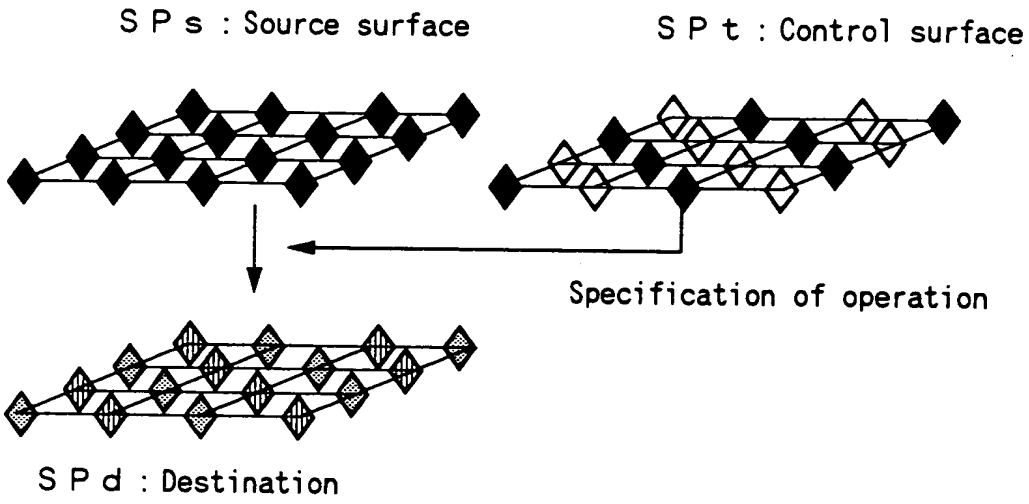

S P s : Source surface
S P t : Control surface
Specification of operation
S P d : Destination

FIG. 20

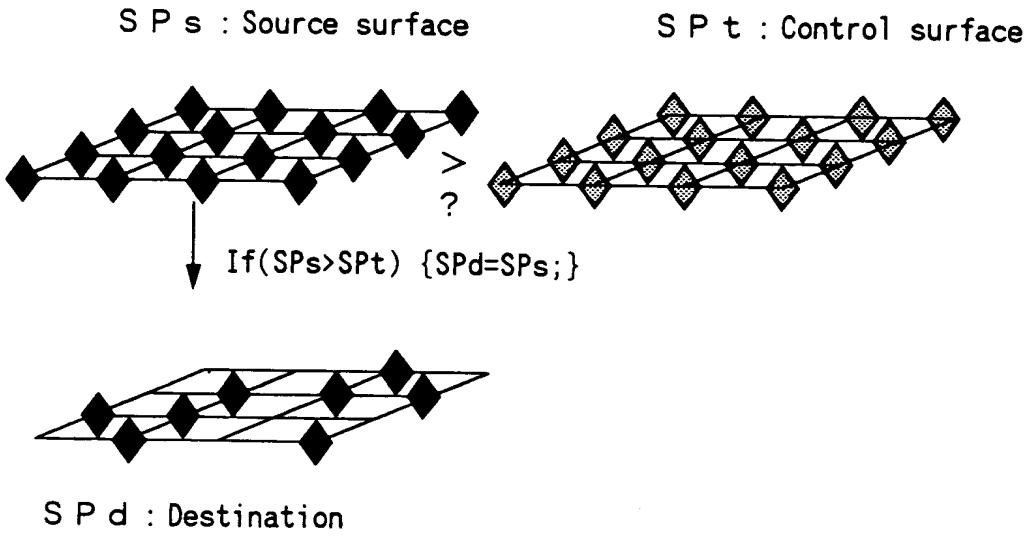

S P s : Source surface
S P t : Control surface
>
?
If(SPs>SPt) {SPd=SPs;}
S P d : Destination

FIG. 21